ABSTRACT

A multi-gate device has a high-k dielectric layer for a top channel of the gate and a protective layer for use in a finFET device. The high-k dielectric layer is placed on the top surface of the channel of the finFET and may reduce or eliminate silicon consumption in the channel. The use of the high-k dielectric layer on the top surface reduces hysteresis and mobility degradation associated with high-k dielectrics. The protection layer may protect the high-k dielectric layer during an etching process.